LISTING OF THE CLAIMS

1. (Original) A central processing unit (CPU) that includes multiple clock zones, said CPU comprising:

in each clock zone,

at least one sensor that generates a power signal indicative of a power supply voltage within said clock zone;

a clock generator for providing a variable frequency clock to said clock zone; and

a controller for controlling an operating frequency of said clock generator in response to said power signal and in response to frequency adjustment communications from other clock zones.

2. (Original) The CPU of claim 1 wherein said controller is operable to communicate adjustments of said operating frequency performed in response to said power signal to other clock zones.

3. (Original) The CPU of claim 2 wherein communication of said frequency adjustments requires at least one clock cycle.

4. (Original) The CPU of claim 3 wherein, when a controller in a first clock zone receives a frequency adjustment communication from a second clock zone, said controller in said first clock zone adjusts an operating frequency of a clock generator of said first clock zone to drive a phase misalignment between said first clock zone and said second clock zone to zero.

5. (Original) The CPU of claim 4 wherein said controller in said first clock zone drives a frequency misalignment between said first clock zone and said second clock zone to zero after driving said phase misalignment to zero.

6. (Original) The CPU of claim 3 wherein a controller in a first clock zone does not communicate an adjustment of an operating frequency in said first clock zone when, in an immediately previous clock cycle, said controller in said first clock zone has received a frequency adjustment communication from a second clock zone.

7. (Original) The CPU of claim 3 wherein a controller in a first clock zone does not perform a frequency adjustment in response to a frequency adjustment communication from a second clock zone when said controller in said first clock zone has performed a frequency adjustment in response to a power signal from said first clock zone in an immediately previous clock cycle.

8. (Original) The CPU of claim 1 wherein said at least one sensor is a voltage detector.

9. (Original) The CPU of claim 1 wherein said at least one sensor is a thermal detector.

10. (Original) A method of operating a central processing unit (CPU) that comprises multiple clock zones, said method comprising:

generating at least one power signal that is indicative of a power supply voltage within each of said clock zones;

adjusting a frequency of a first local clock in a first clock zone of said clock zones in response to a respective power signal from said first clock zone;

communicating said first clock zone frequency adjustment to a second clock zone; and

adjusting a frequency of a second local clock in said second clock zone in response to said first clock zone frequency adjustment.

11. (Original) The method of claim 10 wherein said communicating said first clock zone frequency adjustment requires at least one clock cycle.

12. (Original) The method of claim 11 wherein said second zone frequency adjustment comprises:

driving a phase misalignment between said first clock zone and said second clock zone to zero.

13. (Original) The method of claim 12 wherein said second zone frequency adjustment comprises:

driving a frequency misalignment between said first clock zone and said second clock zone to zero after driving the phase misalignment to zero.

14. (Original) The method of claim 11 further comprising:

receiving, at the first clock zone, a frequency adjustment communication from a third clock zone in a clock cycle immediately subsequent to said first clock zone frequency adjustment; and

omitting adjustment of a frequency of a first local clock of said first clock zone in response to said third clock zone frequency adjustment.

15. (Original) A central processing unit (CPU) that includes multiple clock zones, said CPU comprising:

in each clock zone,

means for generating a power signal that is indicative of a power supply voltage within said clock zone; and

means for modifying a frequency of a respective variable frequency clock in response to said power signal and in response to frequency adjustment communications from other clock zones.

16. (Original) The CPU of claim 15 wherein said means for modifying a frequency communicates frequency adjustments to other clock zones.

17. (Original) The CPU of claim 16 wherein communication of frequency adjustments requires at least one clock cycle.

18. (Original) The CPU of claim 17 wherein a means for modifying a frequency in a first clock zone is operable to drive a phase misalignment between said first clock zone and a second clock zone to zero in response to a frequency adjustment communication from said second clock zone.

19. (Original) The CPU of claim 18 wherein said means for modifying in said first clock zone is operable to drive a frequency misalignment between said first clock zone and said second clock zone to zero after driving said phase misalignment to zero.

20. (Original) The CPU of claim 17 wherein a means for modifying a frequency in a first clock zone does not adjust a variable frequency clock in said first clock zone in response to a frequency adjustment communication from a second clock zone, if the second clock zone frequency adjustment communication is received in a clock cycle that is immediately subsequent to a frequency adjustment performed in said first clock zone in response to a power signal from said first clock zone.